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Users Guide to Intersil's Online "Noninverting Op Amp Designer"

What the Design Tool is Intended to Provide

The tool is intended to accelerate the designers' progress towards a board ready solution in several steps.

1. The designer enters their desired gain, bandwidth and chooses one of 5 optional non-inverting input topologies on "Stepping Through the Requirements Page" on page 2. Next, "Navigating the "Setup" Page" on page 5 the total operating supply voltage may be updated from a default value of 5V and an intended maximum output swing in V_{P-P} can be updated from its default $2.5V_{P-P}$. Finally, the designer can update the default linearity spec from an assumed "Step" response to a design targeting a range of SFDR targets. These two options are used to estimate a required device slew rate to support the linearity specification over the maximum output swing. Click "Apply" on this "Setup" screen to use targets and constraints to screen and rank the available op amps to those that will satisfy the requirements.
2. The tool will attempt to select the minimally suitable part to the requirements, but all other parts that would also work with ascending order of design margin are also listed for selection. All devices that have been rejected are also still available for selection by opening the "Alternate Op Amps" key at the bottom of the list of suitable op amps.
3. With a device part number selected (marked in red at the top right on the setup page), click on "Design" to execute the solution for the resistor values. However, in case of AC-coupled inputs, an input capacitor value is suggested as well.

In the course of the design, the tool will deliver the target gain with a small signal bandwidth and slew rate exceeding the requirements while considering the following:

1. Input bias current cancellation for devices that offer matched input bias currents.
2. The total output noise will not be increased excessively beyond what the selected amplifier noise terms will produce by themselves.
3. Feedback parasitic loading will not interact with the small signal response. This is both an output stage loading consideration and driving point impedance back to device parasitic input C on the inverting node (for Voltage Feedback Amplifier - VFA, solutions)
4. Input DC offset to accomplish bias current cancellation will not present a significant part of the intended input signal magnitude.

Once designed, the tool allows immediate simulation of small signal AC response, step response, and/or output noise. It also provides a re-design feature where the designer can update the feedback R value (and/or the blocking cap value) and then have the tool re-design the other elements using that value. And finally, any design can then be ported to iSim PE where more complete circuit simulations can be executed and/or multiple stages and circuits connected together for larger system evaluation.

There are several design assumptions that have been made to simplify this initial interactive user interface.

1. Complementary Bipolar supplies are assumed in these circuits (Similar to the Active Filter Designer). While single supply designs are very common, the solution algorithms start with bipolar designs then those can be easily adapted to single supply in most cases. See "Appendix A" on page 15 for examples of circuit adjustments to map to single supply solutions. The actual simulation file for a single supply design is easily developed by editing the circuit ported from this tool into iSim PE.
2. The delivered bandwidth will always be something greater than the specified minimum desired bandwidth (sometimes significantly greater depending on the device selected). Since the tool is considering slew rate issues also, it sometimes needs to pick parts that are much faster than the minimum target bandwidth to provide the max $V_{O(P-P)}$ slew rate without limitation. The intention here is to take the desired minimum bandwidth and guardband that somewhat before amplifier selections and design solution are executed. This is primarily intended to build in some production guardband recognizing the simulation model shortcomings. No op amp macromodel attempts to deliver AC responses that account for power supply variation from nominal, operating temperature variations, or process case limits. So it is best to start by targeting some nominally higher number to avoid disappointment later. Many tools insert capacitors to exactly hit the target bandwidth and that is certainly physically possible in the solutions delivered here. In a way, that really becomes a first order filter design tool; not just a non-inverting op amp design tool. "Appendix B" on page 18 steps through the 3 topology choices for adding a single pole filter to the resulting non-inverting designs delivered here. Each has its pros and cons and can be easily tested in the circuits delivered from this tool that has been ported to iSim PE.
3. The tool supports an immense range of possible op amp solutions - from the 35kHz ISL28194 µW Voltage Feedback Amplifier (VFA) to the >500MHz EL5167 Current Feedback Amplifier (CFA). As much as possible, the tool will try to deliver resistor solutions that minimize response peaking in the small signal frequency response. For the VFA devices, this means the feedback loading and phase margin impacts of the values chosen are considered. For the CFA, this means a nominally constant bandwidth Butterworth closed loop response is targeted up through some

maximum gain, then it converts to a Gain Bandwidth characteristic (increasing the Rf value) as the gain continues to increase to avoid excessive loading in the feedback path.

4. No additional output loading or interface network is included. The range of possibilities there is quite large and easily added to the delivered designs ported to iSim PE. A good design practice would be to run the AC response in iSim PE for the original circuit, then add the intended next stage load and re-run to see if any significant impact should be expected.
5. It is quite easy to input a set of targets and constraints that are not realizable with the current product set. For instance, asking for a 40V supply with 30V swing and 100MHz bandwidth at a gain of 50 will come back empty for solutions. The tool will calculate what those targets imply in terms of gain bandwidth product and slew rate, but will indicate no device is available. At this point, you can force a design with a part manually selected using the “Alternate Op Amps" key, but more preferably, reset your targets to something plausible in this physical universe.

All of these assumptions are aimed at delivering a robust solution with some, but not excessive, design margin to the requirements. It does this while offering numerous options and branch points for the designer to test different features and devices in the design.

Stepping Through the Requirements Page

The tool opens with an assumed set of targets and input network. That screen appears as Figure 1 showing the default gain (2V/V), target minimum bandwidth (50kHz), and desired input impedance (10kΩ).

For the Noninverting Op Amp Designer, the specified gain can range from 1V to 100V/V while the target minimum small signal bandwidth can range from 10Hz to 500MHz.

The schematic is a typical non-inverting op amp design where an input termination resistor is defined as Rin (this element becomes very useful if a single supply adaption is desired) and a series element Rb is included. Often, Rb is optional but the designs delivered here include a minimum value of 20Ω. Some value for Rb is very useful in board implementations where

1. If the op amp is a VFA offering matched bias currents, Rb is used to tune the DC source impedance looking out of V+ separately from a defined input impedance.
2. If the op amp is a very high speed bipolar device, a 20Ω right at the V+ inputs will protect the high speed transistor inputs from reactive source Z's that might provoke a parasitic oscillation.
3. Where this stage is driven from the output of very high speed device, a small value for Rb can help isolate that prior stage from the parasitic input capacitance of this stage. This can be an effective way to improve the stability and flatness of the entire signal chain in a board environment.
4. If the inputs can be overdriven or ESD zapped, a simple 20Ω Rb element can go a long way towards limiting fault current magnitudes.

Where none of these conditions apply to the design envisioned, Rb can certainly be eliminated from the schematic. However, recognizing that designs sometimes change over time, with different op amps placed into the board, a place for Rb in the layout might be a good design practice where it could be a 0Ω value when none of the considerations listed previously apply.

The default circuit includes a resistor to ground set to 10kΩ. The allowed range on this Rin is 20Ω to 1MΩ. For design purposes, V_{IN} is assumed to be a 0Ω source (like the output of another amplifier) in this default condition. One option allowed, is to eliminate this Rin and drive directly into Rb. The source is still assumed to be a 0Ω and only Rb is available for bias current cancellation. Also, eliminating Rin removes the option of an AC-coupled input as the input stage bias current can now only be supplied from V_{IN}. Selecting this option gives the screen shown as Figure 2 where both the AC-coupled and source matched options have gone away. If the design is intended for single supply, this option will require the V_{IN} to supply the DC bias within the input range of the device.

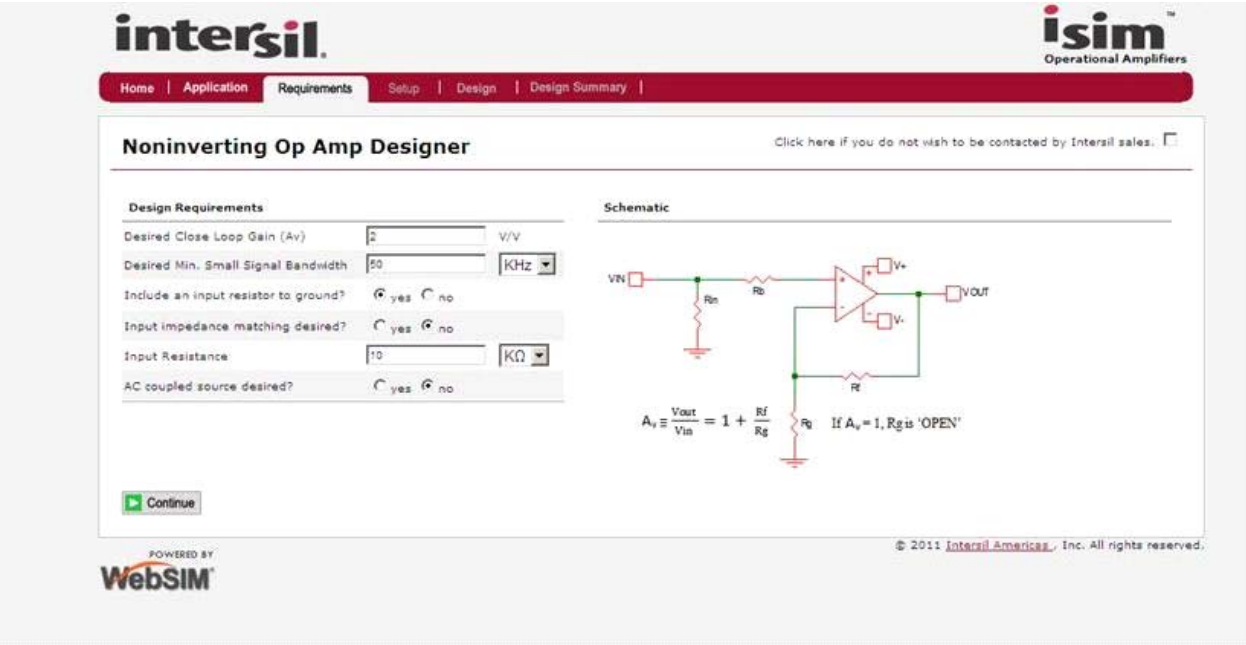

FIGURE 1. DESIGN REQUIREMENTS PAGE WITH DEFAULT SETTINGS

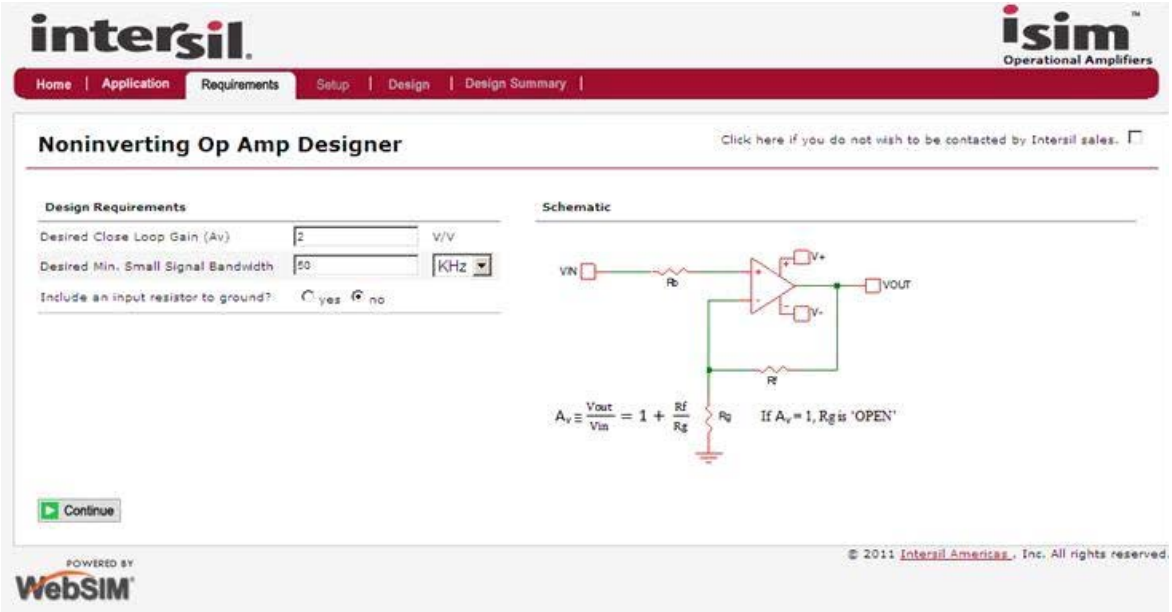

FIGURE 2. NO INPUT RESISTOR TO GROUND SELECTION

Going back to having this input resistor to ground, the remaining two options on the “Stepping Through the Requirements Page” on page 2 are to include a DC blocking cap and/or design for a doubly terminated matched impedance (for higher speed designs). Selecting "Yes" for "AC-coupled source desired" gives the circuit of Figure 3 with default values still in place.

Here, V_{IN} is still assumed to be a 0Ω source for design purposes, but now the DC impedance looking out of the V+ node is going to be Rb + Rin while the AC source impedance will transition to just Rb at frequencies above the high pass pole formed by C1 and Rin (C1 is selected in the design flows to place that high pass pole at approximately 3 decades below the actual high frequency F-3dB, but that can be manually adjusted in the re-design feature provided in “Executing the Design” on page 7). Changing the screen of Figure 3 to select "Yes" for a matched input impedance desired, gives the screen of Figure 4. Here, the input resistance had now defaulted to 50Ω. When a matched input impedance is desired, the allowed range on this Rin compresses to be from 20Ω to 800Ω.

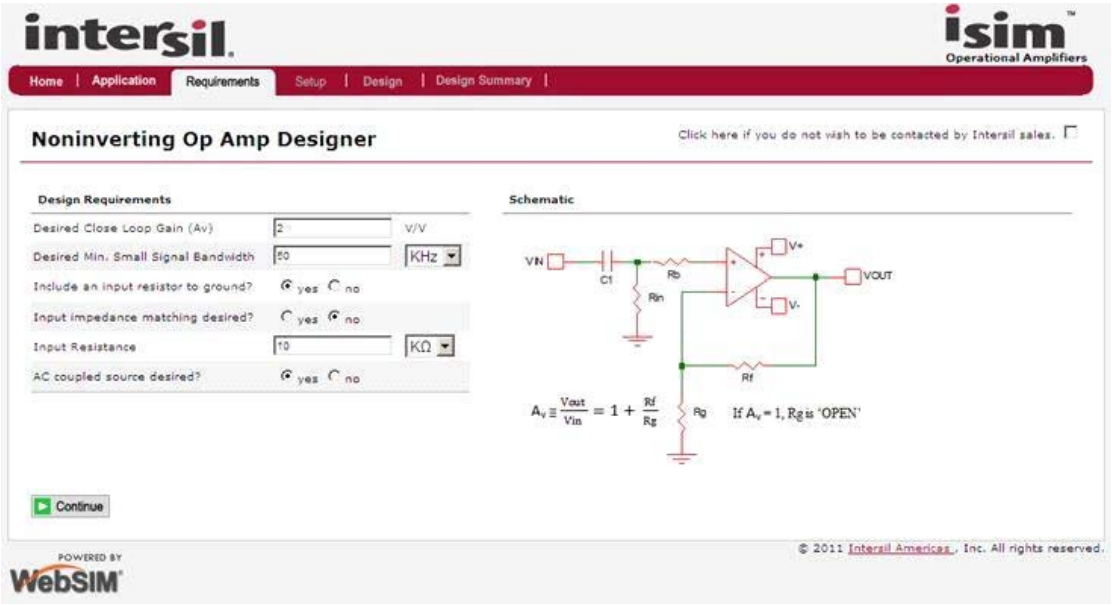

FIGURE 3. AC COUPLED SOURCE SELECTED

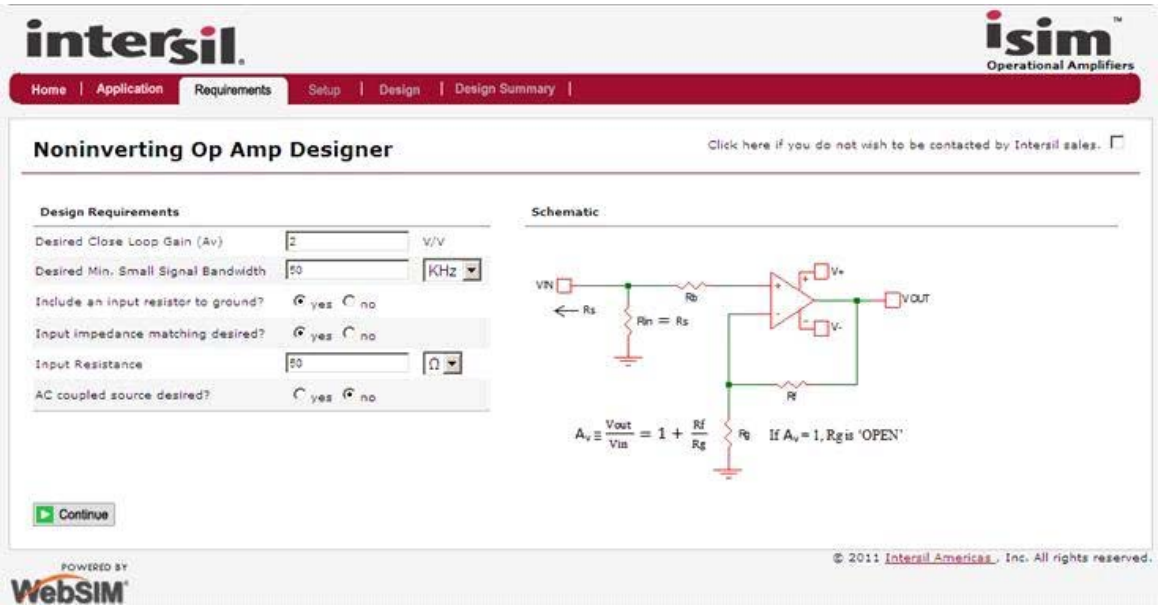

FIGURE 4. AC-COUPLED SOURCE AND MATCHED INPUT IMPEDANCE SELECTED

In this case, the DC source impedance looking out of V+ is Rs+Rb while the AC source impedance flattens out to Rb + Rs/2 at frequencies above the high pass set by C1. And the final input circuit supported by this design tool is a DC coupled, matched input impedance design as shown in Figure 5.

In this design, both the AC and DC source impedances are set to Rb + Rs/2.

Once the input configuration, target gain from V_{IN} to V_{OUT}, small signal bandwidth, and input resistance are selected (when there is an Rin to ground selected), hitting "Continue" will go to the "Setup" page.

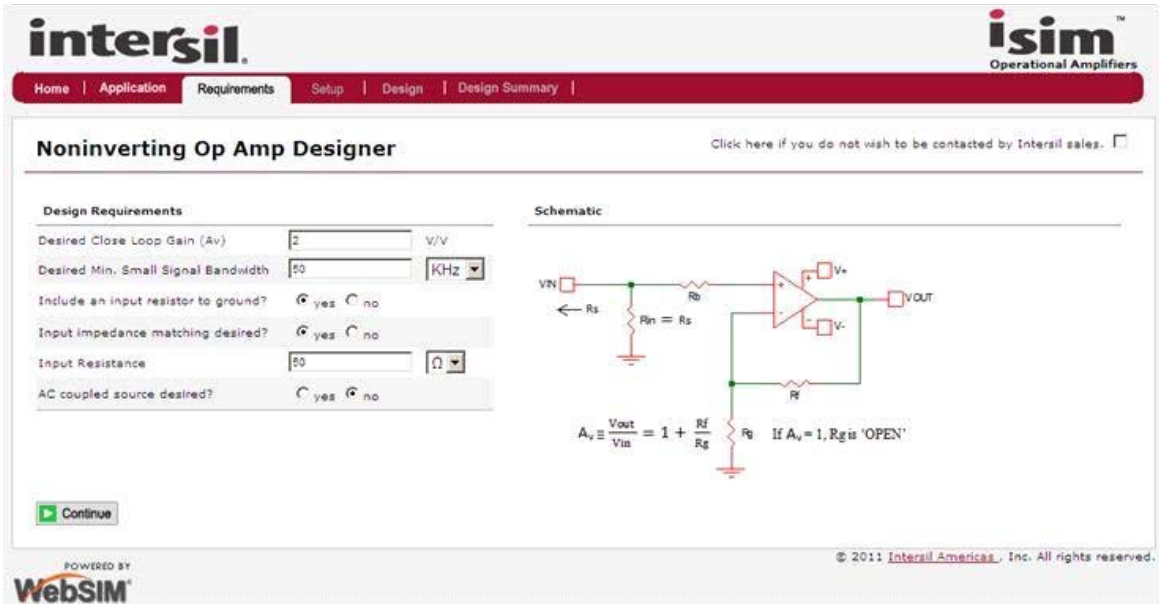

FIGURE 5. DC COUPLED, MATCHED INPUT IMPEDANCE SELECTED

Navigating the "Setup" Page

Going back to the original default design of Figure 1, and hitting "Continue" will take you to the "Setup" page of Figure 6.

On this page, the target requirements are repeated in the upper right, while the "Design Constraints" are in the upper left. These default to a total 5V supply across the op amp (that will be split into ± ½ of this value in the final schematic; so for a ±5V design, enter 10 here), the desired maximum output V_{P-P} swing, and the intended linearity specification. This defaults to a step response where that output swing, and the target bandwidth, are used to estimate a maximum output dV/dT to set a guardbanded minimum device slew rate to avoid non-linear operation. The other option for the linearity specification is SFDR where then a range of targets is provided that will also feed into a guardbanded minimum slew rate requirement to possibly satisfy that SFDR target. And finally, a desired resistor tolerance field is available where it defaults to 1% but allows exact, 0.5%, 1% and 2% values to be used in the design. Entering new values in any of the design constraints fields will require the "Apply" key to be pressed to update the computed requirements and re-screen for amplifiers.

Each of these fields has an allowed range.

1. Supply voltage may range from 1.8V to 40V
2. Maximum output V_{P-P} defaults to 0.5*Total supply voltage, with an allowed range between 10% and 90% of the Total supply voltage. The 90% limit is intended to avoid clipping for full scale swings or steps when the design is delivering a 2nd order frequency response. It is certainly possible to intend a design to drive the full supply range on the outputs, but this setup page will not accept those entries.
3. For the "Step" linearity specification, nothing else is required. Changing the maximum output V_{P-P} will change the target minimum slew rate directly.
4. Switching to the "SFDR" linearity specification opens up two new fields. A target SFDR that defaults ranging from "60dBc to 69"dBc for a maximum output frequency. Thus, defaults to 50% of the target small signal bandwidth and the maximum frequency intended for the SFDR target can also be overridden to be within a range of 10% to 80% of the target minimum small signal bandwidth. Also, a drop down list of SFDR ranges allows either higher or lower targets to be entered. At very high targets, a significant margin in the amplifiers required output slew rate will be required vs the signals' maximum slew rate (at max output V_{P-P} and frequency). This slew rate margin calculation provides a "necessary but not sufficient" condition for achieving a desired SFDR. Executing a design with a device offering the target slew rate margin increases the chance of hitting the SFDR range, but the final performance depends on too many variables to capture in this initial design flow. Refer to the specific target device data sheet for more detailed information on loading issues, distortion over gain issues, etc.

The default page shown in Figure 6 has already taken the target requirements and constraints, calculated some required slew rates and bandwidths, screened the available Intersil op amps, and ranked them by order of ascending design margin. Here, the ISL28136 appears as the closest fit and has been selected for "Design" (the red part number in the upper right area). Any of the other devices listed at the bottom may also be selected for design by clicking the "Select" key next to it. Clicking on the red part number will take you to the "Device Information Page" where the different packaging and full data sheets would be available.

The design tools work with the base single channel version of a product family. The multichannel and/or disable versions of these single channel options will be reported in the design summary if those are more desirable options for the end application.

In getting to the list of candidate solution devices, the Setup page has screened the possible devices for the following:

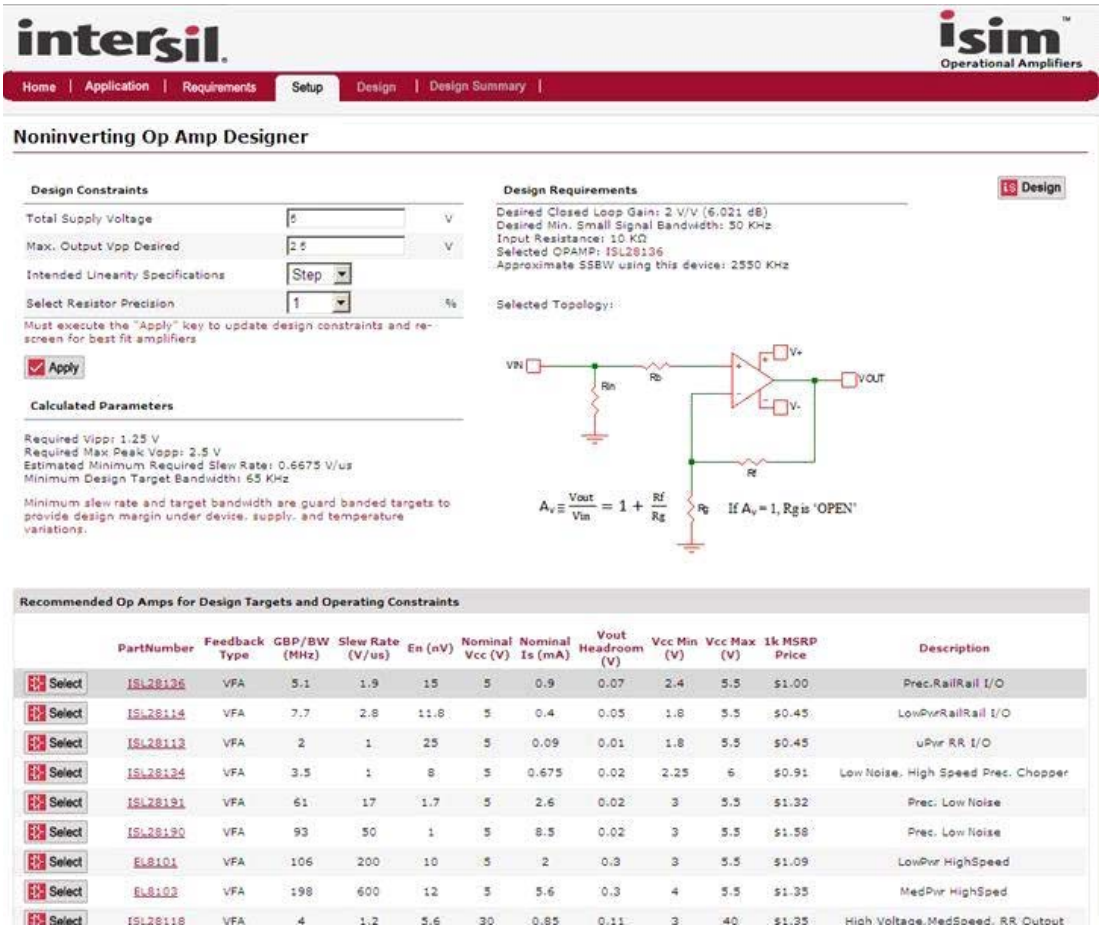

FIGURE 6. SETUP PAGE USING THE DEFAULT SETTINGS

1. Desired total supply voltage can be supported by the device.
2. Desired maximum output swing at that total supply can be supported (output headroom checked).
3. Required maximum input swing can be supported (input headroom checked).
4. Device will be stable at the target gain and can provide ≥ 1.3x the target minimum small signal bandwidth at the desired gain.
5. Device offers at least the computed required minimum slew rate. This is guardbanded 2X in the step linearity choice and a varying amount in the SFDR linearity choice. To remove this as a constraint, choose the lowest SFDR linearity target at the minimum frequency (10% of target SSBW).

While these screening parameters will certainly get a reduced subset of possible solutions, it is not intended that they provide the only device that can be used in the design tool (top one listed and the default selection, ISL28136 in the default design flow). For that reason, the "Setup" page lists all the remaining devices deemed suitable at the bottom (of Figure 6) with a short list of critical parameters that might be of interest to the designer. These include the following:

1. Feedback type - both VFA and CFA devices are available in the tool where the VFA will have a gain bandwidth product while the CFA will generally be much higher in frequency vs quiescent power with reduced DC precision over VFA.
2. Gain bandwidth product if VFA or gain of 2 BW if CFA. This gives an indication of design margin to the desired targets. For any device selected, the estimated closed loop bandwidth with that device is also computed and reported in the upper right of the "Setup" screen. Since the Intersil device macromodels include excellent internal parasitic and 2nd order modeling, the actual simulated bandwidth will only approximately match the simple calculation used in the upper right of the "Setup" page.
3. Slew Rate - this will often be the limiting constraint (vs bandwidth) on the proposed solution devices. Looking at the example of Figure 6 using the ISL28136, the estimated closed loop bandwidth of 2550kHz far exceeds the guardbanded target of 65kHz but the available slew rate of 1.9V/µs is just above calculated target of 0.67V/µs. The design tool is often not able to exactly match all required targets and constraints and instead sorts in ascending design margin from the parameters of the available devices.
4. Input voltage noise for the op amp. This parameter is not used to screen or rank solution options. However, once a device is selected, the solution algorithms will attempt to control the noise added by the resistors to be a minor contribution to total output noise vs. the noise contribution of the op amp terms themselves. So, if output noise is of principal concern, pick the lowest noise device in the screened amplifier list - in Figure 6, that would be the ISL28190. Doing this often comes

at the cost of more quiescent current so that is also listed in the table so the designer can trade off this noise vs quiescent power issue.

5. Nominal supply voltage and supply current at that nominal voltage, and supply voltage range helps the designer recognize where his design is in the available operating range and universe of devices.
6. 1k MSRP pricing is also listed - be sure to check the device information page for the most recent list pricing.

Following the list of tool screened and ranked devices are a key for "Alternate Op Amps". Pressing that will expand a list of every part available in the design tool that has been screened out to the current design targets and constraints. These are simply listed in VFA then CFA in ascending bandwidth order. This feature is very useful to test the effect of choosing unsuitable devices for the design.

These design tools and macromodels do not detect if the simulation is operating at a supply voltage outside the available range for the device. They will correctly limit for the I/O voltage swings, but a device rated for instance at a maximum 5V supply will simulate fine if operated at for instance ±15V (in simulation, not in physical reality). If the designer chooses to design from the Alternate Op Amps list, they must carefully verify that the operating supply voltage matches that supported by the device. Those devices in the screened list have already been verified to this parameter.

Executing the Design

Hitting the "Design" button at the upper right or lower left will take the desired targets and selected device and execute the design for the feedback and gain resistors as well as the Rb element. Doing that from the default page of Figure 6 gives the design shown in Figure 7.

The design has zeroed in on a 1kΩ feedback resistor value and, since the ISL28136 offers matched input bias currents, it has also adjusted the Rb element to the required 499Ω value to get an improved output DC offset. The 499Ω is the closest 1% value to the exact 500Ω that would mathematically be required. The design algorithms principally focus on the feedback resistor value, where, for the VFA design flows it is considering

1. Noise added by the resistors should not dominate the output noise. In the circuit of Figure 7 this includes the Rb element where it will be adding a 2.8nV/√Hz term to the 15nV/√Hz of the ISL28136 voltage noise term for instance.
2. The effect of the total feedback loading is considered. There, the Rf + Rg appear as a load in this design and both a maximum current for the specified maximum output V_{P-P} is checked as well as a minimum loading before the frequency response is impacted through op amp output impedance. For this default design, the ISL28136 is looking for something ≥2kΩ load before 2nd order output impedance issues start to impact the small signal frequency response giving increasing deviation from a gain bandwidth calculation. That consideration has in fact set the Rf value in the example of Figure 7.
3. The feedback network will also introduce a parasitic pole to the inverting input C that is being considered in the solution algorithms. If too low in frequency vs the estimated closed loop bandwidth, this will introduce phase margin loss in the design leading to peaking and possibly unstable performance and a ringing step response.
4. The Rb calculation is also bounded by the parasitic pole to the V+ parasitic capacitance (AC source impedance consideration).
5. The I/O DC offset introduced by the bias currents are also considered and controlled to a low level to avoid unintended I/O clipping due to these DC error issues.

From the design delivered, several options are available on this page. Across the top are 3 possible simulations that can be run: Step response, small signal AC response, and output noise simulation. The "Configure" button allows you to customize those simulations. On the upper left, 3 vertical tabs give you the choice of the following:

1. Returning to this page of choosing the simulations
2. The pages of simulation results
3. A re-design option where you can choose the Rf and/or blocking cap value and re-run the design and simulations.

In the lower left of the Design output page is the related multi-channel or disable version devices. Also, the schematics show split bipolar supplies with no de-coupling capacitors. In implementation, those are required with values depending on the device selected. Refer to the device data sheet for recommendations.

By clicking "AC Analysis" it runs a small signal AC simulation giving the response of Figure 8.

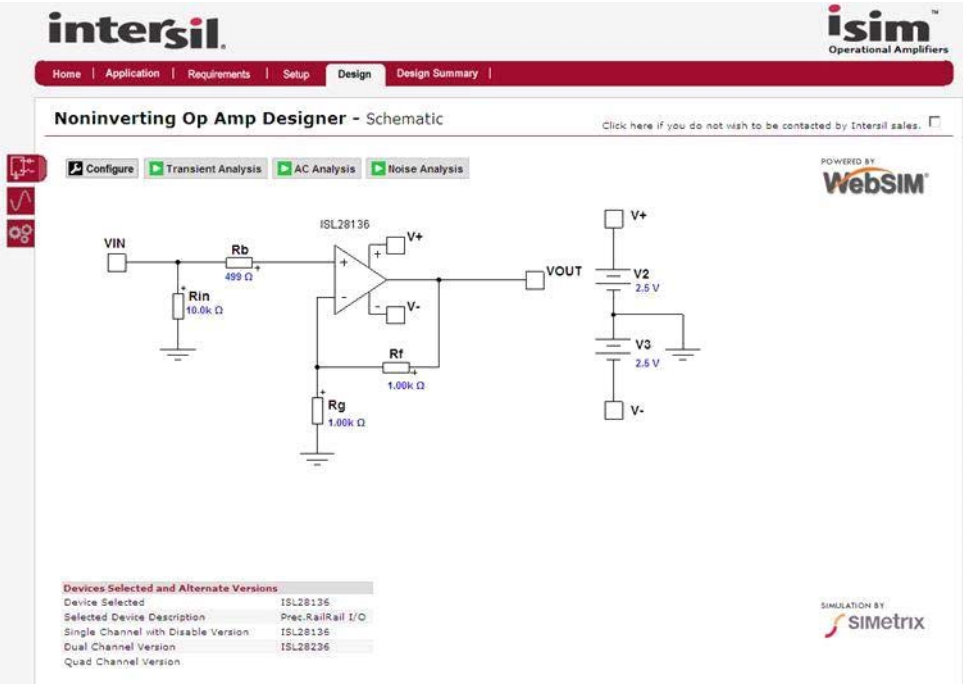

FIGURE 7. DESIGN DELIVERED FROM THE DEFAULT DESIGN FLOW

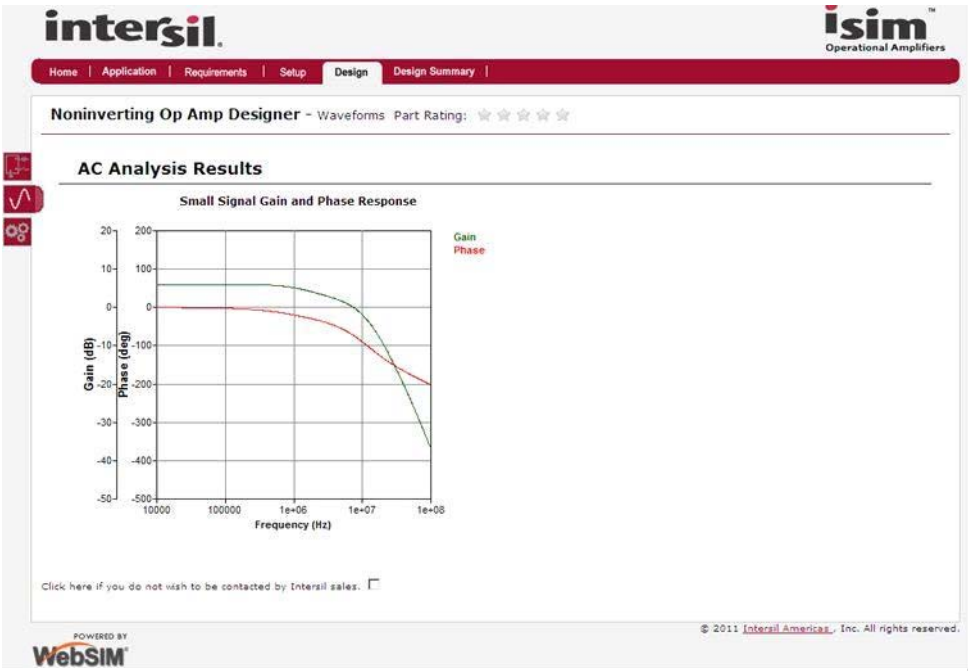

FIGURE 8. AC RESPONSE OF THE DEFAULT DESIGN

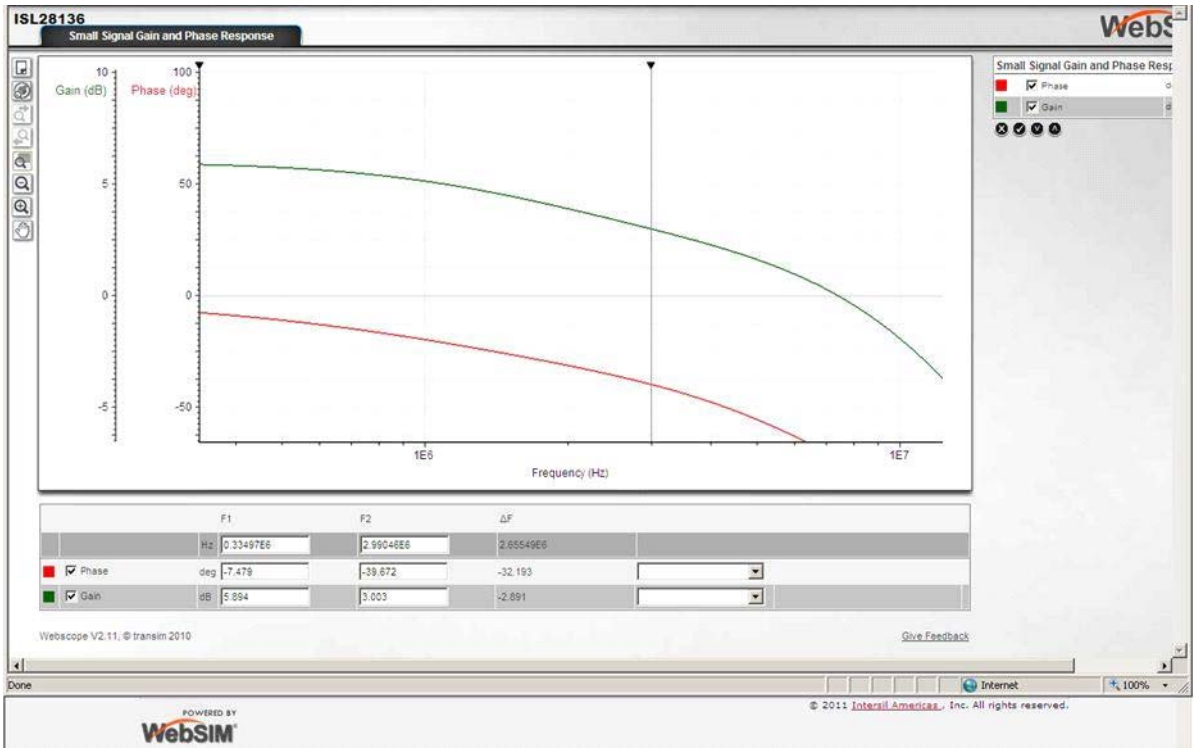

FIGURE 9. WAVEFORM VIEWER SHOWING THE -3DB POINT ON THE F2 MARKER

So this shows the expected low frequency gain of 6dB with what looks like a well controlled 2-pole rolloff. The first pole approximately sets the F-3dB point but the models are including (and showing) some higher frequency effects as well.

Double clicking on any of these simulation plots within the iSim tools will open a waveform viewer where zoom and marker functions are available.

In Figure 9, the waveform viewer has been opened and the F2 marker moved to 3dB gain. Here it is showing a 2.99MHz -3dB frequency, close, but not exactly, the approximate 2.55MHz predicted in the setup page. Again, the calculation on the setup page is a first order calculation while the simulation models include numerous parasitic elements intended to more closely predict actual device performance. Adding a capacitor to set the F-3dB is certainly possible and Appendix B steps through the 3 choices and their pros and cons.

Manually Changing Values or Using the Redesign Feature

In the "Design" page, double clicking any of the external elements that show a value in "Blue" will open up a window to change those values. This is not going through any of the solution algorithms but simply allowing the designer to manually set everything (except the selected op amp, go back to the setup page for that).

The lowest of the 3 red tabs along the upper left of Figure 8 (the gears) is a path to a redesign feature within the tool. Pressing that, from the default design of Figure 8, gives the following screen. Here, the feedback resistor (Rf) may be changed as well as the desired resistor value tolerances. This proceeds in 3 steps

1. First enter a new resistor value and/or tolerance selection
2. Hit the Calculate key and a table of proposed new values will be displayed using the design algorithms encoded into the tool.
3. If those are acceptable, hit the "Apply" key and the schematic will be updated

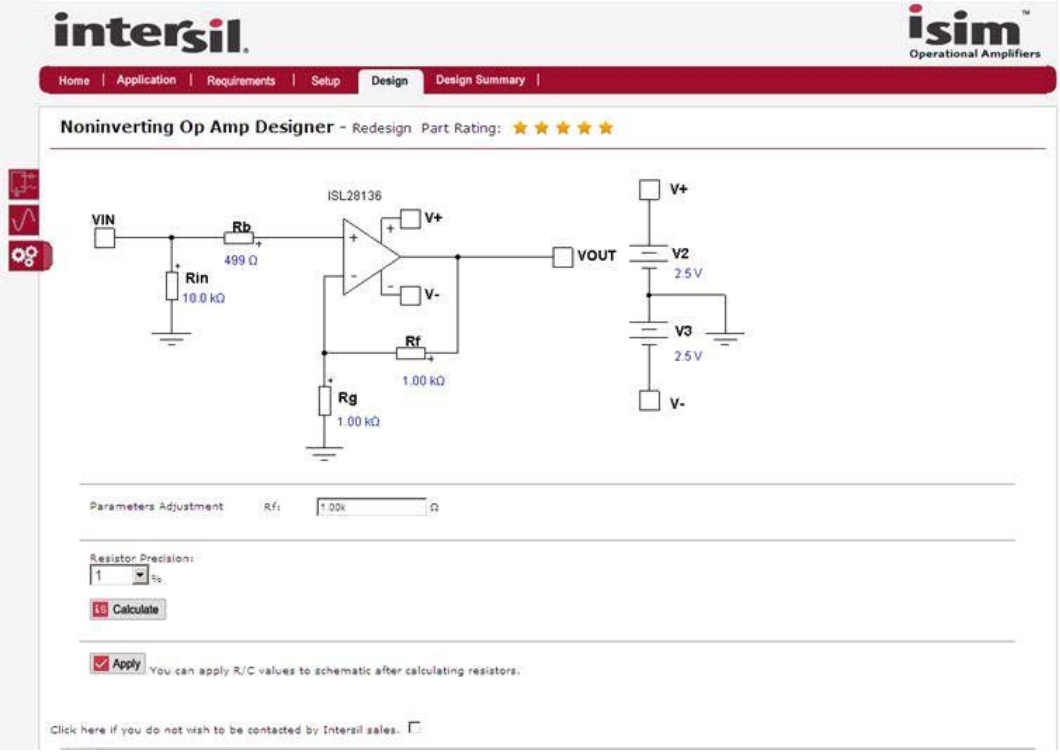

FIGURE 10. REDESIGN PAGE FROM THE DEFAULT DESIGN WITH THE ISL28136

Redesigning for a 5kΩ Rf and 1% value snap gives the following schematic.

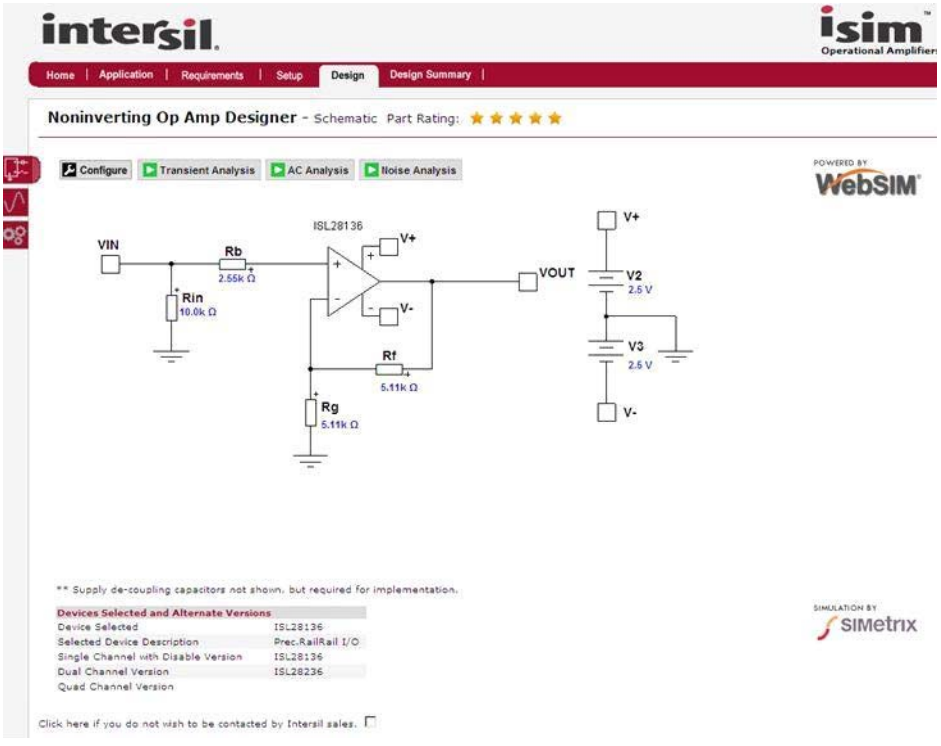

FIGURE 11. RE-DESIGNED FOR A 5kΩ FEEDBACK R_f

Re-running the AC Analysis now will show the impact of these higher resistor values interacting with the parasitic input C of the ISL28136 (1.5pF is in the model). This circuit now has a pole in the feedback set by the 2.55kΩ driving point impedance to the V-node and that 1.5pF parasitic (board layout parasitics would add to this). That 41MHz pole is adding some phase shift around the feedback loop which definitely impacts the small signal frequency response. Compare this response to the nominal design with 1kΩ feedback in Figure 8.

The added phase shift has increased the Q for the op amps closed loop poles adding a slight peaking which has extended the -3dB point to about 7MHz. With the increased Rb resistor (for bias current cancellation), the signal response also now has a 40MHz simple pole to the V+ node due to the same 1.5pF parasitic on that node. This can be seen in the approximately 3-pole rolloff above 20MHz in the simulated response of Figure 12. However, these higher resistors have also increased the output noise and added a higher peak in the spot output noise - following this stage with a simple RC is very effective at reducing that effect. The simulated spot output noise for this re-designed circuit is shown in Figure 13.

Here the spot noise is starting at about 35nV/√Hz (very close to 2X the op amps 15nV/√Hz input voltage noise term) but then peaks to about 280nV/√Hz. This same plot using the 1k = Rf starts out at 30nV/√Hz and then peaks to 170nv/√Hz.

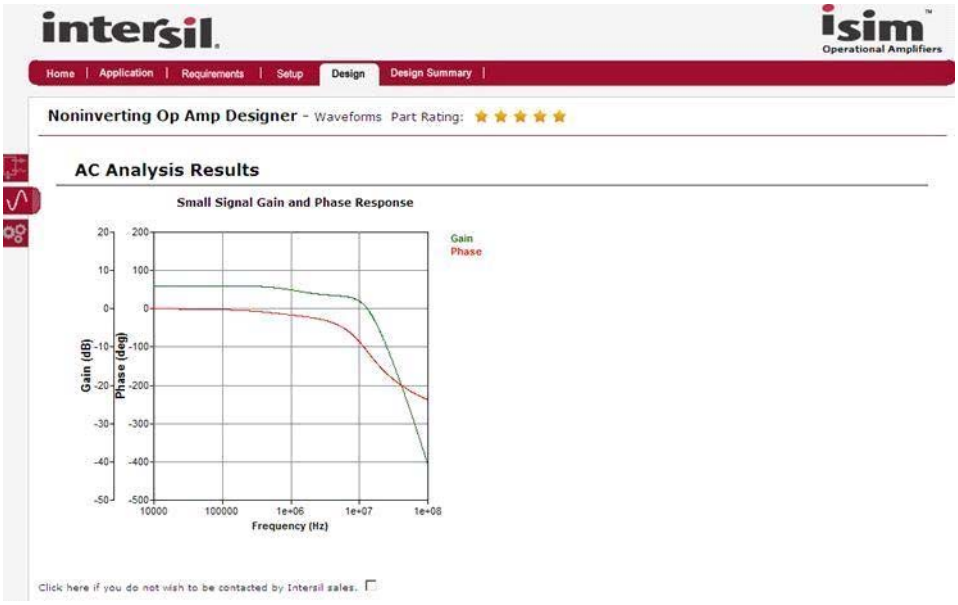

FIGURE 12. REDESIGNED FREQUENCY RESPONSE WITH R_f = 5.11kΩ

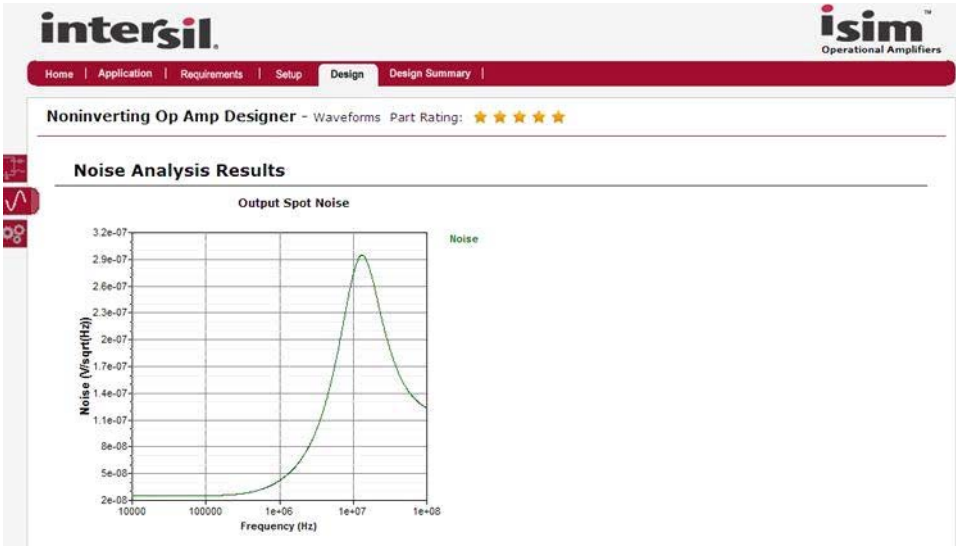

FIGURE 13. SPOT OUTPUT NOISE WITH R_f = 5.1kΩ REDESIGN

Comparative plots are not supported in the "Noninverting op amp designer" directly. Those are most easily generated in iSim PE where superimposing plot outputs is the standard plot mode.

Going back to the screen of Figure 8 on page 8 and pressing the "Design Summary" key will give you Figure 14. Here the targets and device information are summarized with 2 more options in the upper right of this screen.

The entire summary and simulation results can be downloaded to a pdf file by pressing the "PDF Download" key in the upper right of this page. This makes it very easy to share or document proposed designs. The other key "Download Schematic" ports the design into a much more complete simulation environment called "iSim PE" where PE is Personal Edition. A circuit file ported and saved into iSim PE then also gives an easy way to save and share design files within that environment. This software must first be loaded locally on the designer's computer and from that point forward, schematics ported into that environment are local and not served. It is in this environment that easy circuit editing is possible - changing designs to single supply, adding bandlimiting caps or loading elements, as well as concatenating designs chains together. The current version of iSim PE is available from the Intersil design tools landing page.

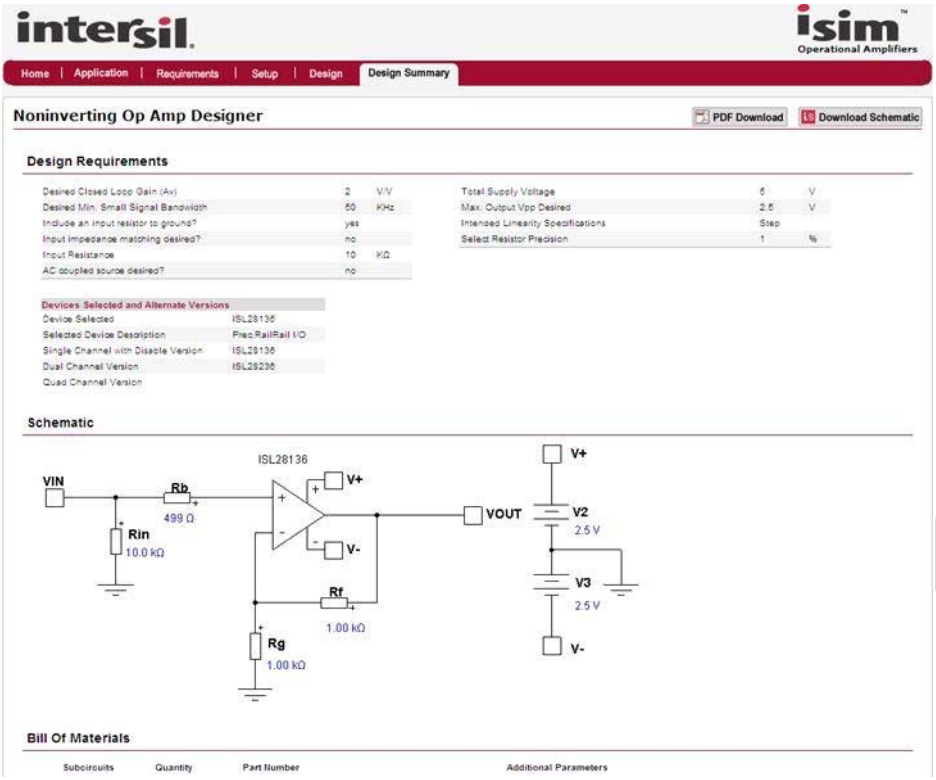

FIGURE 14. DESIGN SUMMARY PAGE FOR THE DEFAULT DESIGN

Designs Ported to iSim PE

Hitting the "Download Schematic" button in the upper right from the Design Summary tab of Figure 14 will take you to this page (if iSim PE has been loaded onto your local computer).

Here, the simulation has added DC probe points showing nominal input and output DC offsets. The source comes in set up to run the full transient, AC and noise simulations but that can be changed under the "Simulator" key. The full scope of capabilities found in iSim PE is beyond the scope of this document but an introductory application note is available as AN1652, "iSim:PE User's Guide"

http://www.intersil.com/data/an/an1652.pdf

Here, it is very easy to add elements and even change the op amp used in the design. Double clicking on the op amp symbol will open the entire list of Intersil op amps available within the iSim PE library. These are the same models available as text files on the device information pages but compressed in the design tools and iSim PE library to use fewer simulation nodes. This allows larger circuits to be easily built up out of these common building blocks circuits delivered from the online tools. Appendices A and B use this tool to generate the single supply and bandlimiting options from this initial circuit. Schematic editing capability is not provided in the online tools, but the component values can be highlighted and changed while within the online environment. In the local iSim PE environment, double clicking on an element opens up a window to change the value. Running the original small signal frequency response simulation for the circuit of Figure 14, and then changing to the redesign values of Figure 10 and re-running will give this comparative frequency response where the extended bandwidth one in Figure 15 is with the R_f = 5.11kΩ.

Recalling that the original target bandwidth in this example design was only at least 50kHz, adding a simple RC pole after the Rf = 1kΩ design, will give the simulation circuit of Figure 16. To limit the added loading of this filter, a 5kΩ series R into a 160pF simple RC pole will add a pole to the overall response at 200kHz.

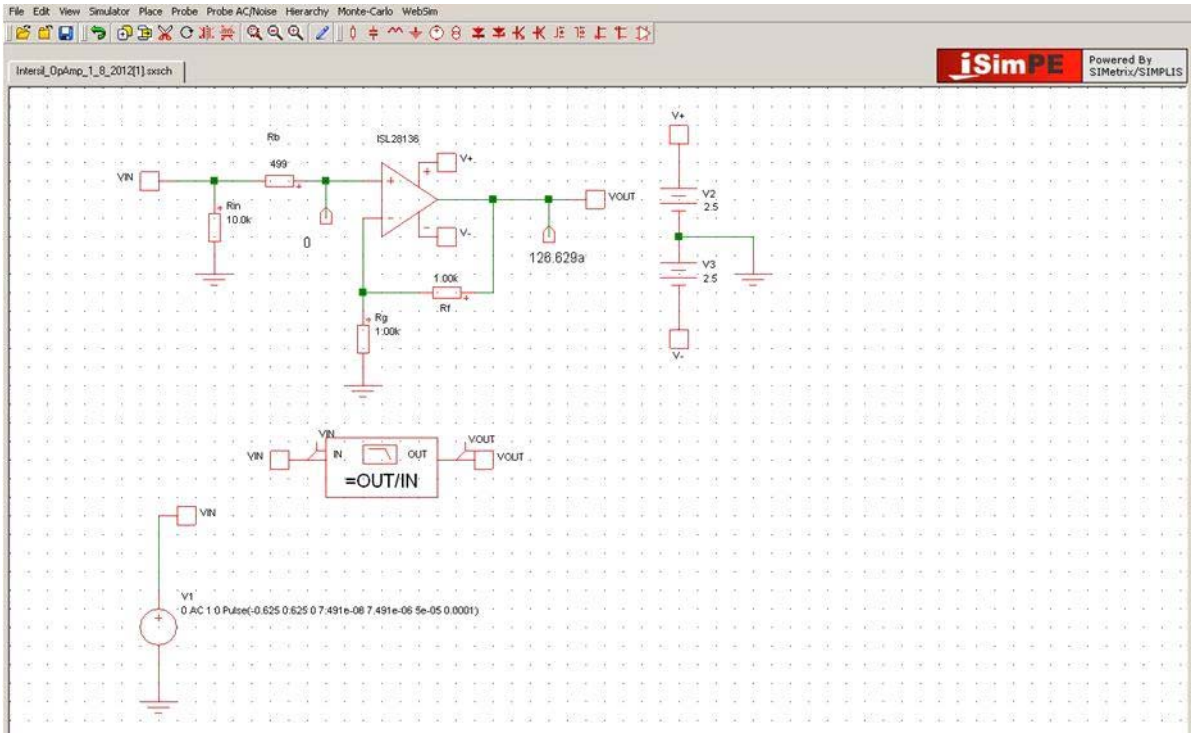

FIGURE 15. iSim PE SCHEMATIC OF THE DEFAULT DESIGN PORTED FROM THE NONINVERTING OP AMP DESIGNER

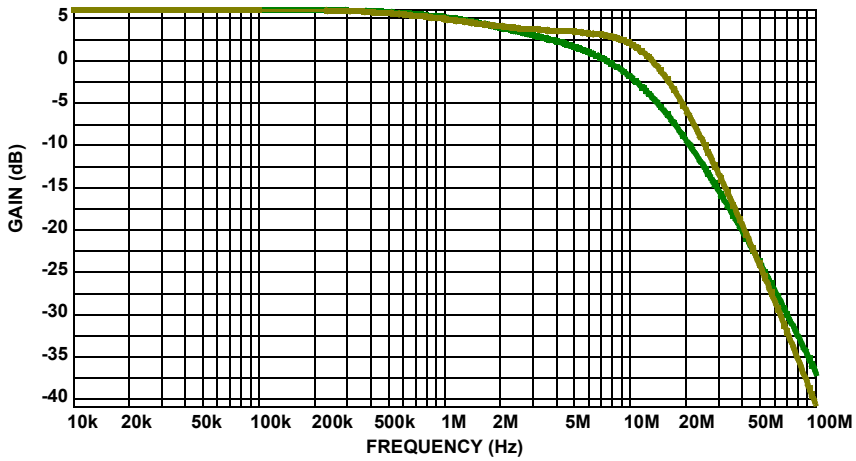

FIGURE 16. COMPARATIVE FREQUENCY RESPONSE PLOTS IN iSim PE

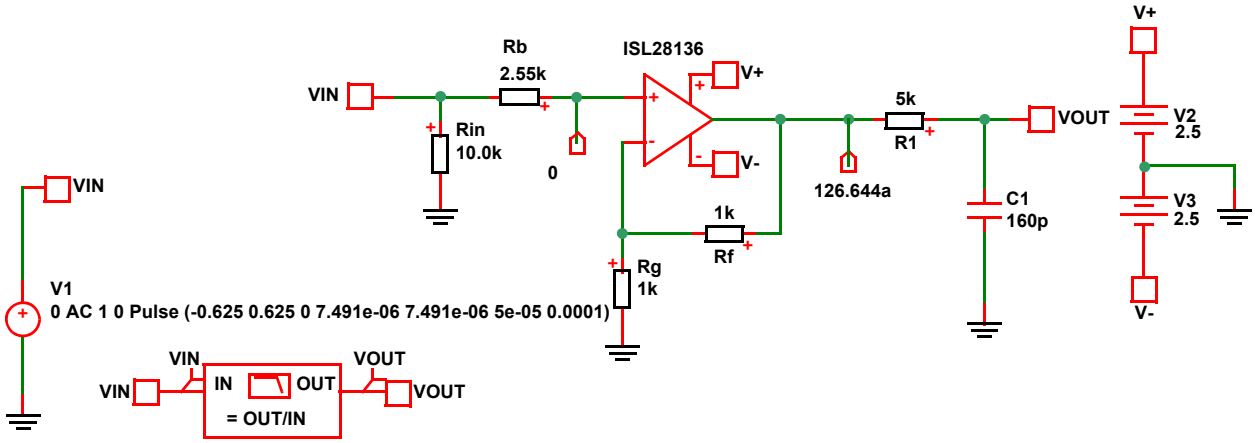

FIGURE 17. MODIFIED SCHEMATIC IN iSim PE WITH A 200kHz POST RC TO CONTROL OUT OF BAND NOISE

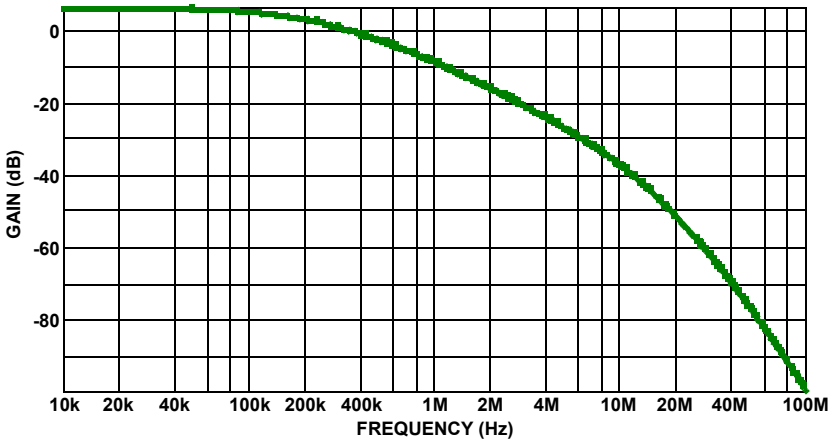

FIGURE 18. SIMULATED SMALL SIGNAL FREQUENCY RESPONSE WITH 200kHZ POST FILTER ADDED

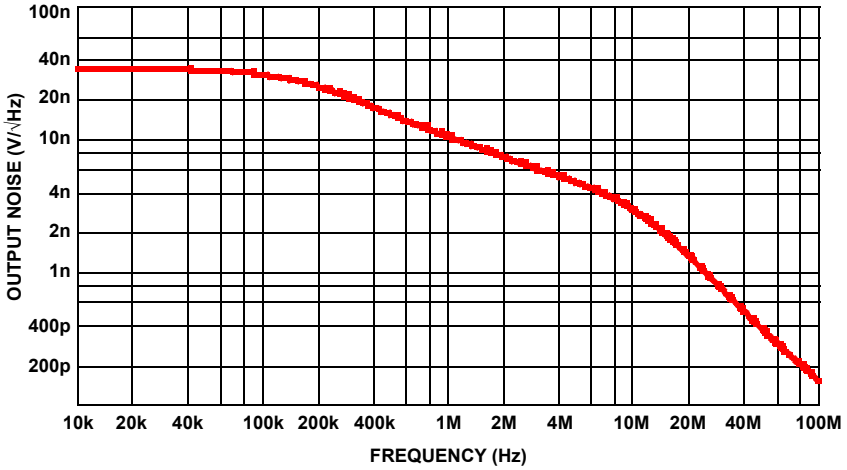

FIGURE 19. SIMULATED OUTPUT SPOT NOISE IN ISIM PE FOR THE POSTFILTERED DESIGN OF FIGURE 17

This type of simple post (RC pole) will also remove the noise peaking in the original design as shown in Figure 19.

Here, instead of a peaked output noise over frequency due to the slight noise gain peaking inside the original design, we see a well rolled off output noise. It is this type of "what-if" analysis that is easily performed with the iSim PE design tool starting from proposed designs ported from the iSim op amp tools.

Summary

Intersil's "Noninverting op amp designer" provides an easy to use, single stage, design tool that partially automates a portion of the design engineers' task. Given performance targets and systems constraints, it narrows the list of possible devices to quickly and effectively achieve the design goals while considering a large range of 1st and 2nd order issues. It then delivers proposed external element values that are also considering an expanded range of 1st and 2nd order issues. Considerably, flexibility in overriding these design flows is also provided giving the designer an easy means to exercise and test their own designs using the broad range of Intersil's precision and high speed op amps. For the most complete and capable design environment, these tool generated circuit blocks can also be ported to a full Spice simulator for further analysis and iteration.

Appendix A: Example Adjustments from Dual Supply to Single Supply

Starting again from the default design, some simple approaches to single supply operation are shown here.

Topology A: Split supply this is Rin to ground, DC connected V_{IN}, and an Rb resistor to adjust for Ib cancellation. The Bipolar ±2.5V supply version of this solution is in Figure 20A.

Making V2 = 5V and V3 = 0V will be more suitable for a single supply +5V solution. Essentially, this requires the DC operating voltages to all remain in this 0V to 5V supply range for the amplifier to work properly. Since the ISL28136 is a rail-to-rail input and output device, V_{IN} from 0V to 2.5V can be directly connected in a single +5V version of this circuit at a gain of 2. Another approach is to assume V_{IN} has a DC level in range, and then a small signal of interest on top of that. Then, if a good low impedance version of that DC level were available, tying the RG_S2 and RG_S1 to that reference can give a DC-coupled single supply solution.

More often, going single supply is done by AC coupling the input to the a supply midpoint and then inserting a DC blocking cap in series with RG_S1 as shown in Figure 20B.

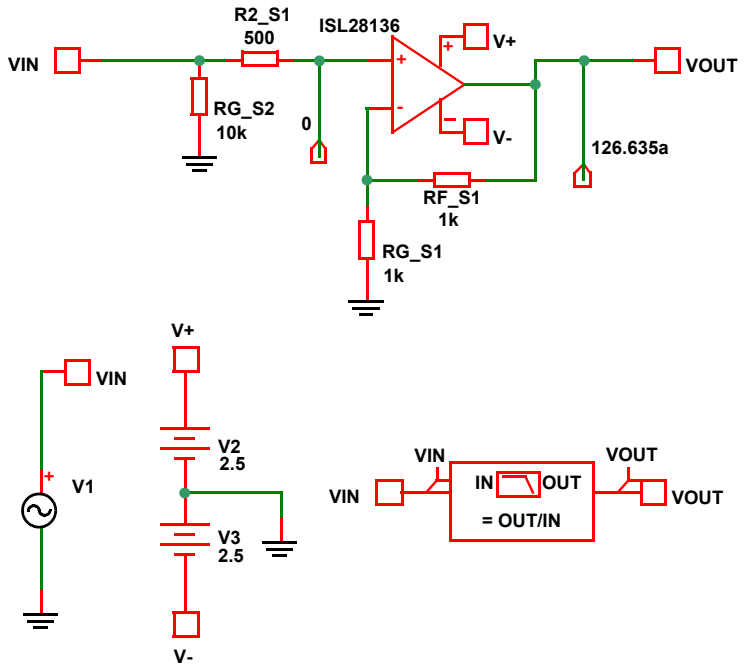

FIGURE 20A. DEFAULT TARGETS AND ISL28136 SOLUTION FROM THE ISIM PE SIMULATION FILE

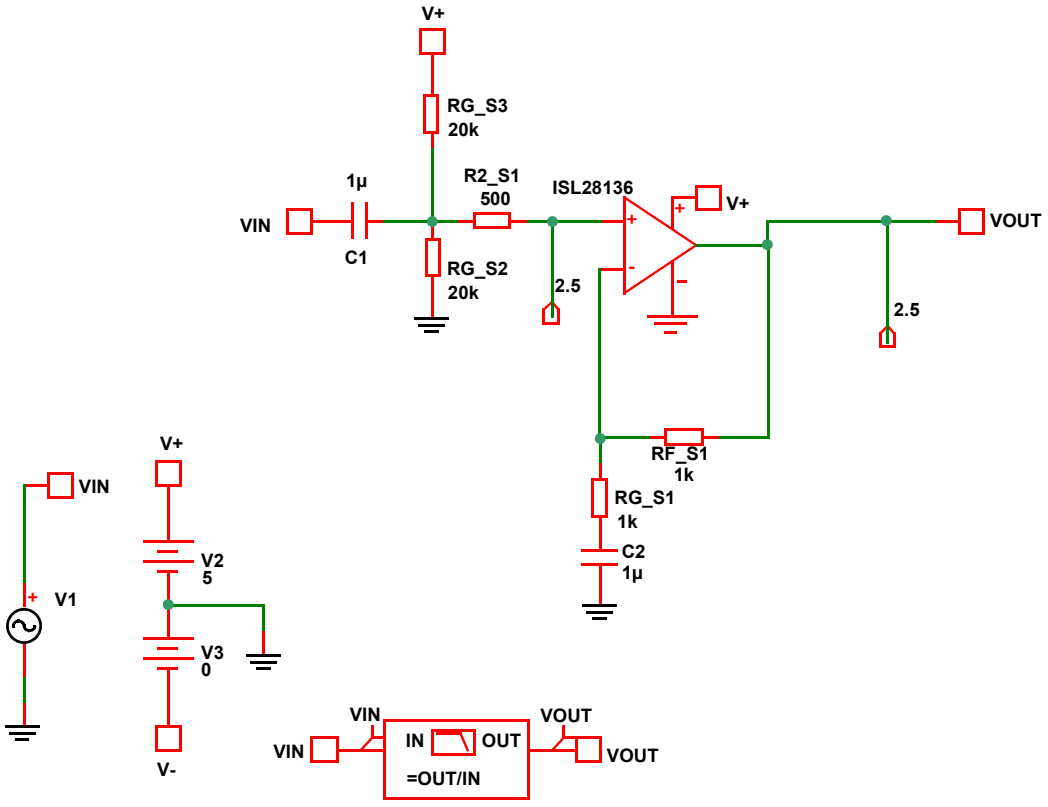

FIGURE 20B. SIMPLE CONVERSION TO SINGLE SUPPLY FOR TOPOLOGY A

The DC probes at the V+ input and V_{OUT} show a 2.5V DC operation. Doubling the original Rin resistor value and using 2 of them off the single +5V supply provides the midpoint DC bias with the same midband input impedance (10kΩ). One added consideration with this approach is the DC gain for the two input bias currents has changed considerably from Figure 20A. So any Ib gain matching effort in the original design will need to be reconsidered. Also, the supply voltage now shows up as an input to the circuit to the extent that the source is not really a 0Ω source over all frequencies. If the design is headed towards single supply and AC coupling the input is acceptable, it is best to choose one of the AC input options on the "Requirements" page. Then, the circuit just needs the DC blocking cap in series with Rg to make it single supply (C2 in Figure 20B).

A comparison of AC responses for Figures 20A and 20B appears in Figure 20C. The high frequency response rolloff is identical (F-3dB at 3MHz) while the single supply version introduces a high-pass pole at about 115Hz using the 1µF blocking caps as shown in Figure 20B.

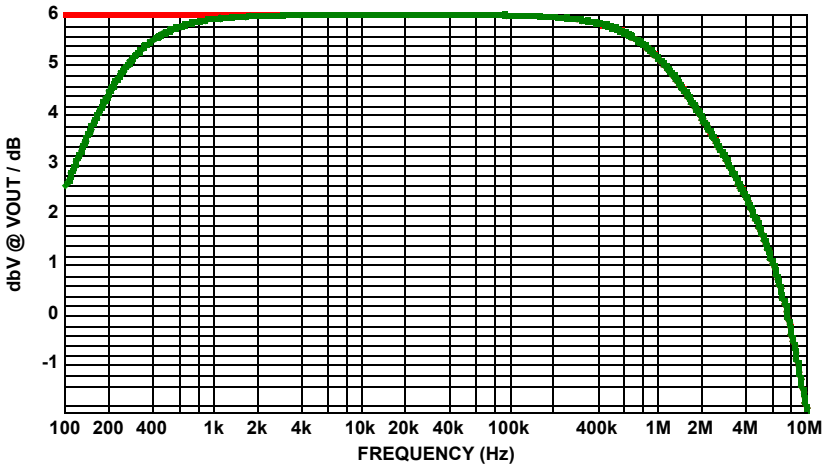

FIGURE 20C. DUAL AND SINGLE SUPPLY AC RESPONSE CURVES

Appendix B. Adding a Controlled F-3dB to the Non-inverting Op Amp Design

Any op amp by itself will be giving a bandwidth that is modestly controlled over temperature and from part to part. The designs here are aimed at making sure that bandwidth is comfortably beyond the design target while also considering slew rate, I/O limits, etc. Many designers then use 1 of 3 techniques to set a more precisely control signal bandwidth in the non-inverting design. These are:

1. Adding an input cap to the V+ input to filter the original signal to a known bandwidth.
2. Adding a feedback cap across the Rf resistor to set a pole on the signal gain.
3. Adding an RC filter at the output to make a final bandwidth control on the full circuit.

Using the default circuit in iSim PE (Figure 14) that has been used throughout this discussion, we will add a 200kHz first order pole in each of these 3 places and then compare frequency response and output noise effects. Figure 21A shows adding a 200kHz RC pole at the input.

This will certainly give a more controlled overall frequency response. Some pros and cons are as follows:

1. Need an Rb value that keeps the cap value reasonable. Here, the bias current cancellation R was not adding much noise in band, so the cap value is reasonable.
2. On very high speed devices, a cap right at the input can sometime impair input stage stability. Often, adding a 20Ω in series to ground with the cap will fix that. That then introduces a minimum attuation as the divider between that 20Ω and the Rb value.
3. The cap will reduce the noise impedance for the V+ current noise. It will not however do anything to bandlimit the op amp voltage noise to the output. It will also bandlimit the Rb noise and V_{IN} source noise.
4. Limiting the signal bandwidth right at the input helps ensure the output dV/dT stays as low as possible.

Figure 21B shows the 2nd approach of adding a feedback capacitor across the Rf element. This is an extremely common technique that does not work as well as might be expected. This approach essentially transitions the amplifier gain from its low frequency value to a gain of 1. In the example used here that is simply going from a gain of 2 to a gain of 1; not really that much attenuation.

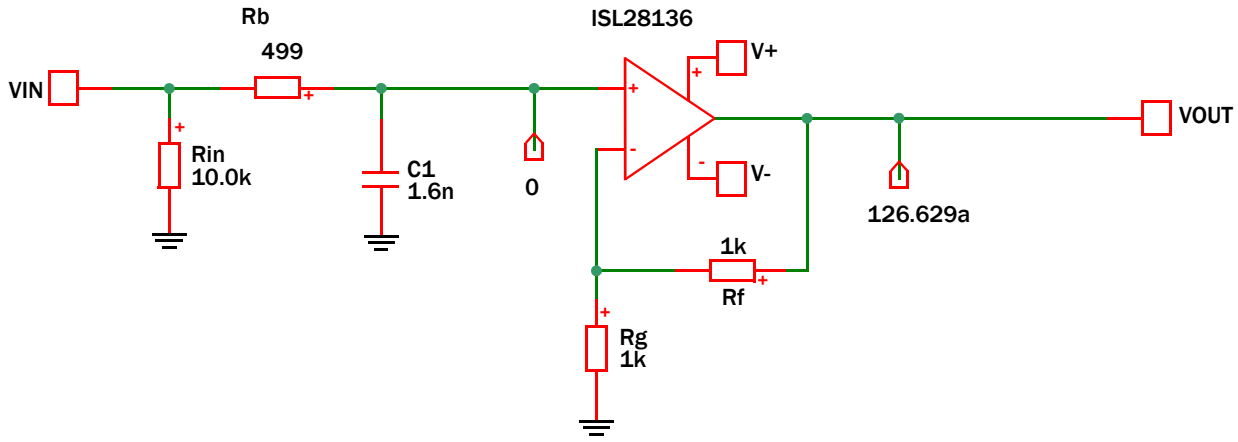

FIGURE 21A. ADDING A SIMPLE RC POLE AT THE INPUT

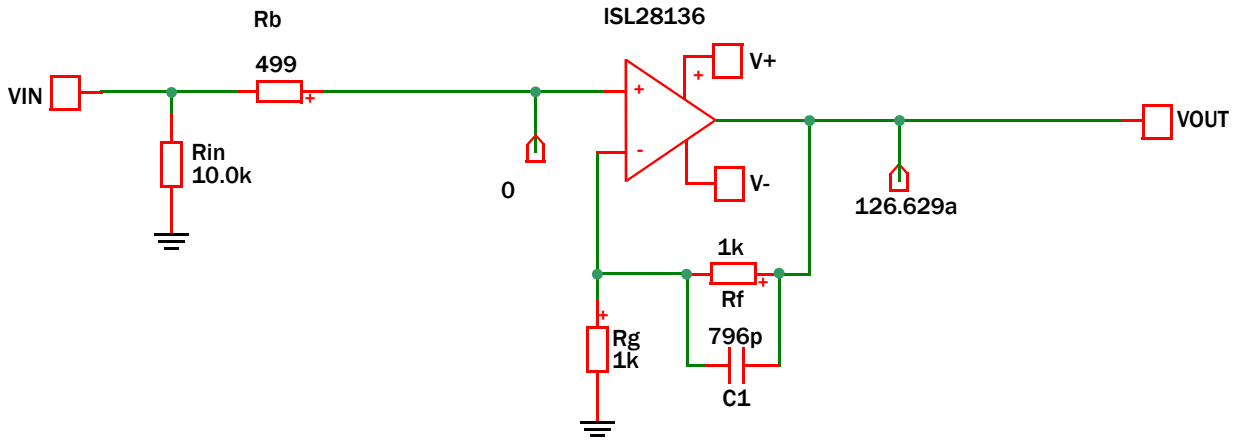

FIGURE 21B. ADDING A FEEDBACK CAPACITOR TO CONTROL THE SMALL SIGNAL BANDWIDTH

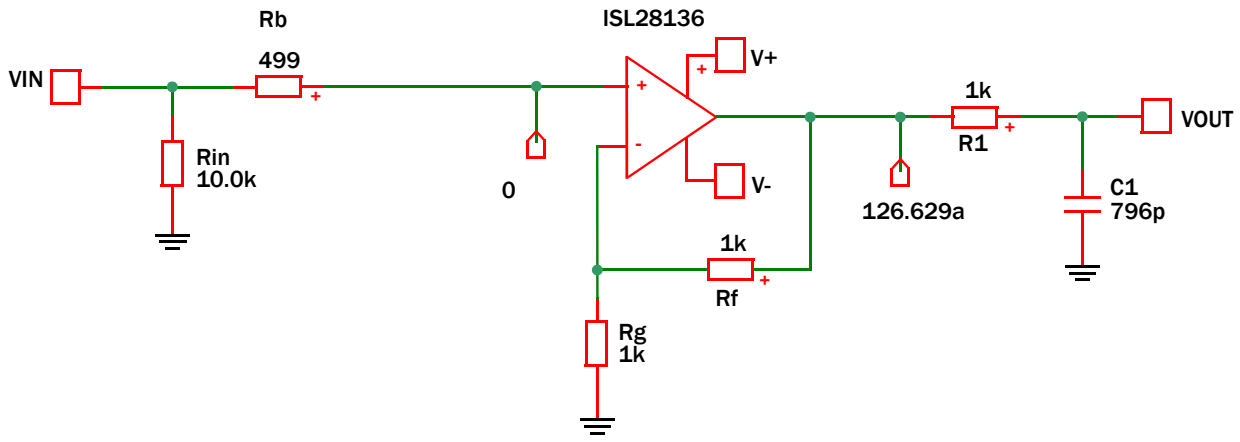

FIGURE 21C. ADDING A 200kHz RC POLE AT THE OUTPUT OF THE AMPLIFIER

Some of the pros and cons of this approach include the following:

1. Both source and load are now isolated from this bandwidth control feature
2. It will roll off the noise contributions somewhat. For the non-inverting terms they will reduce down to a gain of 1, while the inverting side terms get continued rolloff as the C1 impedance of Figure 21B continues on down.
3. This approach cannot (easily) be used with CFA implementations or with non-unity gain stable VFA devices. Both of those limitations can be overcome with added elements but those techniques will also come at the cost of increased output noise
4. For the signal path, the bandlimiting really only continues down to a gain of 1. Using either input or output RC filters will continue the rolloff down below that.

The 3rd option is to place an RC at the output of this amplifier as shown in Figure 21C.

This approach filters everything from the source and op amp before it gets to V_{OUT}. Some pros and cons of this approach include:

1. It does now require 2 elements to be added (instead of just a C). Here, setting that to the tool recommended Rf value will keep the loading and noise of this network in an acceptable region.
2. The next stage may not want to see this capacitive source impedance
3. Extremely fast transitions at the input node will now try to make it through the amplifier before bandlimiting at this postfilter
4. This approach will normally not interact with the amplifier excessively and both CFA and decompensated VFA devices can use this.

So now consider the comparative simulations of the original circuit (with no capacitive set 200kHz pole) and the 3 options shown here.

Figure 21D shows the 4 small signal frequency response curves. Note the feedback C approach has not really introduced much of a bandlimit. This approach becomes more effective for higher nominal gain designs.

So the input and output pole approaches give essentially the same response and by far the most controlled frequency response. The feedback C is taking the gain to 1 (0dB) then the overall amplifier response rolls off from there as it hits its unity gain bandwidth (approx. 51.MHz). These kind of comparison efforts are very easy to execute in iSim PE. That tool also allows plot data to be exported to excel in ASCII for easy plot manipulation and comparisons.

Figure 21E shows the output spot noise comparisons for the different options.

Both the original and an input C show about the same output noise. This is showing the internal noise gain peaking of this low gain application and the result of designing to make the op amp input voltage noise the dominant term. If the Rb resistor were excessively high, these curves would show a difference with the C at the V+ input as it rolls off that resistor noise term. The feedback C helps a little bit for output noise but clearly the most effective is the RC at the output if controlling broadband noise is of interest.

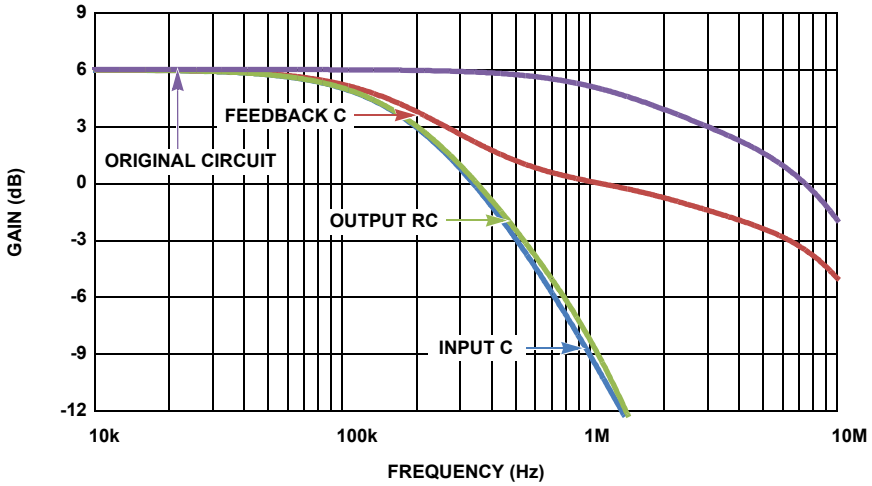

FIGURE 21D. COMPARISON OF THE FREQUENCY RESPONSE FOR THE ORIGINAL AND 3 BANDLIMITING CHOICES

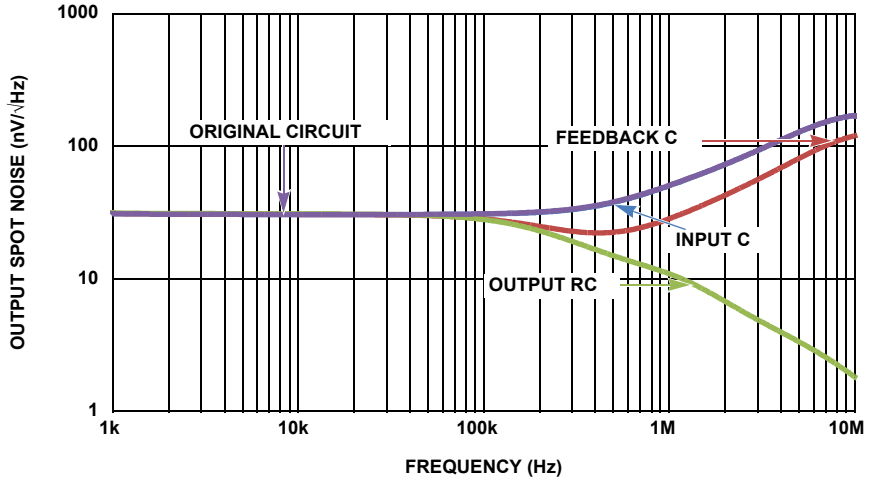

FIGURE 21E. OUTPUT SPOT NOISE SIMULATIONS